PATENT ABSTRACTS OF JAPAN

(11)Publication number:

09-200014

(43) Date of publication of application: 31.07.1997

(51)Int.CI.

H03K 17/00 H01L 27/04

H01L 21/822 H03K 3/02 H03K 19/00

H03K 19/0175

(21)Application number: 08-010175

(71)Applicant:

TOSHIBA CORP

TOSHIBA INF SYST JAPAN CORP

(22)Date of filing:

24.01.1996

(72)Inventor:

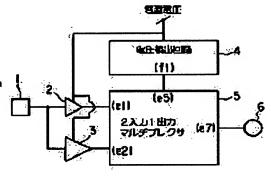
ISHIMOTO SHINJI FUKUDA HIDEKI

(54) SEMICONDUCTOR INTEGRATED CIRCUIT

(57) Abstract:

PROBLEM TO BE SOLVED: To allow a circuit to select automatically with an optional setting of a power supply voltage by connecting each input to plural input buffers and selecting any of the plural input buffers in response to an output signal from a voltage detection circuit.

SOLUTION: An input of an input buffer 2 having a prescribed drive capability with a power supply voltage set to 5V and an input of an input buffer 3 having the same drive capability with a power supply voltage set to 3V are connected to an I/O pad 1. Then an output of the buffer 2 connects to an input e1 and an output of the buffer 3 connects to an input e2 of a 2-input 1-output multiplexer circuit 5. Then an output f1 of a voltage detection circuit 4 providing an output of a digital signal with a level '0' with a power supply voltage set to 5V and providing an output of a digital signal with a level '10' with a power supply voltage set to 3V connects to a selector terminal e5 of the circuit 5. When the circuit 5 receives a level '0' from the circuit 4, the circuit 5 selects the terminal e1 and when the circuit 5 receives a level '1' from the circuit 4, the circuit 5 selects the terminal e2. Then either of the buffers 2, 3 is selected automatically.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

(18)日本四种介介 (JP) (12) 公開特許公報 (A)

(11)特許出數公閱番号

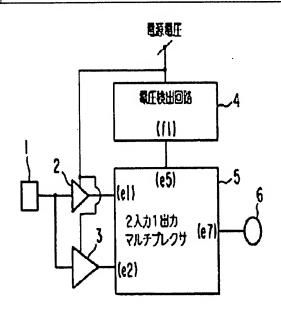
特開平9-200014

(43)公朔日 平成9年(1997)7月31日

(51)IntCL*		識別配号	广内整理番号	FI							技術表示箇所
HOSK	17/00		9184-5K	H03	K I	7/00				H	
HOIL	27/04				:	3/02				P	
	21/822				ľ	19/00		Α		Α	
нозк	3/02			H01	L 2	7/04				F	
	19/00						В				
			審查請求	来簡求	的求明	日の数8	OL	全	6	E)	最終貝に絞く
(21)出頭器(·	特顯平8-10175		(71)世	政人	000003	078				
	-					株式会	让來芝				
(22) 山崎日		平成8年(1996)1			神奈川	県川崎	市中	区集	UILET	72倍地	
				(71) H	人规则	391016	358				
						水芝情	軽シス	テム	长到	会社	
				1		神奈川	果川崎	市川市	A D	日進	町7番地1
				(72) 59	明省	石本	借二				
						神楽川	果川崎	帝市	医 埃	DIE.	580番1号 株
						式会社	東芝半	事件	シフ	テム	技術センター内
				(72) 59	明者	福田	英樹				
						東京都	渋谷区	千駄	ケモ	18	自50番11号 明
						星ピル	米芝	情報	シフ	トテム	株式会社内
				(74) (A MORA	弁理士	AS-TT	武	200		

(54) 【発明の名称】 半導体集積回路





EST AVAILADLE







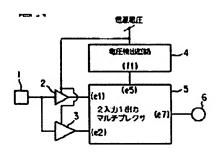


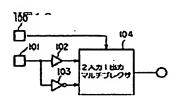


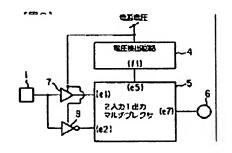


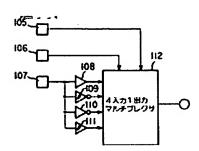


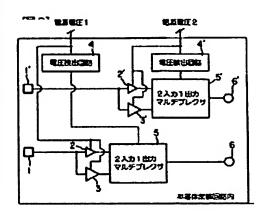
區電腦組織外的

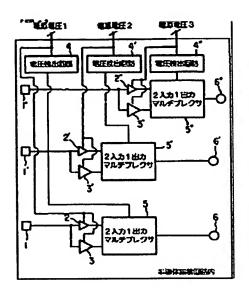


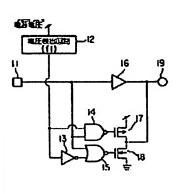


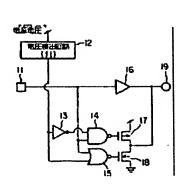


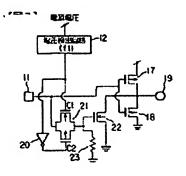


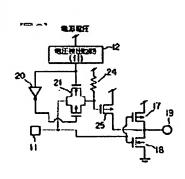


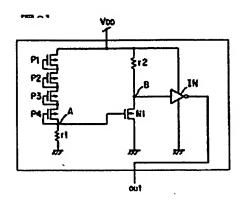












海州系统英母 7878 亮 **国**知記